



VIT

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

REG.NO.:

SLOT:E2

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING CONTINUOUS ASSESSMENT TEST - II FALL SEMESTER 2025-2026

Programme Name & Branch : M.Tech. (Integrated)(MIC,MID)
 Course Code and Course Name: CSI1002 & Operating System Principles
 Faculty Name(s) : Dr.V.Ezhil Arasi, Dr.N. Sivakumar, Dr.G.Manikandan
 Class Number(s) : VL2025260102455, VL2025260102457, VL2025260102459
 Date of Examination : 09.10.25
 Exam Duration : 90 minutes
 General instruction(s):

Maximum Marks: 50

- Answer All Questions
- Course Outcomes:
CO4. Apply and analyze communication between inter process and synchronization techniques.
CO5. Implement page replacement algorithms, memory management and to apply the file system techniques.

Q. No	Answer all the Questions	Marks	CO	BL															
1.	A system has 4 processes (P0-P3) and 3 resource types (A, B, C). The current state is shown below: <table><tr><th>Process</th><th>Allocation</th><th>Maximum</th></tr><tr><td>P0</td><td>0 1 0</td><td>7 5 3</td></tr><tr><td>P1</td><td>2 0 0</td><td>3 2 2</td></tr><tr><td>P2</td><td>3 0 2</td><td>9 0 2</td></tr><tr><td>P3</td><td>2 1 1</td><td>4 2 2</td></tr></table> Available = (2, 1, 0) Analyze whether the system is in a safe or unsafe state. a) If unsafe, determine which process (or combination) could lead to potential deadlock and justify with step-by-step reasoning. b) If safe, consider that Process P1 makes the following resource request (1,1,0). Use the Resource Request Algorithm to determine: • Whether this request can be safely granted, or • Whether P1 must wait, by verifying all algorithm conditions and performing a provisional allocation test.	Process	Allocation	Maximum	P0	0 1 0	7 5 3	P1	2 0 0	3 2 2	P2	3 0 2	9 0 2	P3	2 1 1	4 2 2	10	CO4	BL3
Process	Allocation	Maximum																	
P0	0 1 0	7 5 3																	
P1	2 0 0	3 2 2																	
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P3	2 1 1	4 2 2																	
	In a smart factory, two types of robots, Robot A and Robot B, share a common assembly platform. Robot A functions as a producer, placing a component onto the platform, while Robot B acts as a consumer, assembling and removing the component once it is available. The platform is designed to hold only one component at a time, which requires careful synchronization between both robots to ensure smooth operation. Write a pseudocode using semaphores to coordinate the actions of Robot A and Robot B. Your implementation should prevent race conditions, buffer overflow, and buffer underflow. Use appropriate semaphore variables and clearly indicate where wait() and signal() operations are used. Include explanations with your code to justify how your synchronization logic ensures correct and deadlock-free execution.	10	CO4	BL4															
	a) An IoT gateway node uses Best Fit for large processes (>200 KB) and First Fit for smaller ones. Given free memory blocks [100, 300, 50, 250, 200] KB and incoming processes [P1=180, P2=70, P3=260, P4=90],	5																	



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Question:

1. Apply this hybrid allocation strategy step by step.
2. Show the allocation results and free block status after each request.
3. Comment on how this hybrid approach balances allocation speed and fragmentation control.

b) A database server runs four transactions — T1, T2, T3, and T4 — each holding and requesting certain data locks as shown:

Transaction	Currently Holding	Requesting
T1	X(A)	X(B)
T2	X(B)	X(C)
T3	X(C)	X(A)
T4	X(D)	—

Apply your understanding of deadlock recovery techniques and answer the following:

- a) Identify the transactions that are part of the deadlock cycle and the transactions that are unaffected.
- b) Propose a recovery plan to resolve the deadlock.
- c) Justify your chosen method by discussing its impact on system throughput and data consistency.

4. A computer system uses a cache to speed up memory access. The cache access time is 10 ns, and the main memory access time is 100 ns. If the cache miss rate is 5%, calculate the Effective Access Time (EAT). Also, briefly discuss how the increasing miss rate affects the overall system performance.

b) A computer system uses a 2-level paging scheme with a 32-bit logical address. The page size is 8 KB, and each page table entry requires 4 bytes.

1. Determine how many bits are used for:

- a) Page offset,
- b) First-level page number, and
- c) Second-level page number.

2. Calculate the total memory required to store all page tables if the entire logical address space is utilized.

5. In a satellite communication network, five satellites attempt to transmit data to Earth using shared transmitters arranged in a circular topology. Each satellite requires two transmitters simultaneously (its left and right) to establish a transmission link. If neighbouring satellites attempt to use the same transmitters at the same time, signal interference occurs, potentially halting communication. Design a synchronization mechanism with mutex locks to coordinate the satellites' transmissions safely. Write pseudocode showing how each satellite acquires and releases transmitters using mutex locks. Also, justify how your solution ensures mutual exclusion, avoids deadlock and prevents starvation.

CO5 BL3

CO5 BL3

CO4 BL4