

**VIT**Vellore Institute of Technology  
(Deemed to be University under section 3 of UGC Act, 1956)

REG.NO.:

SLOT: A1

**School of Computer Science Engineering and Information Systems**  
**CONTINUOUS ASSESSMENT TEST - I**  
**WINTER SEMESTER 2024-2025**

Programme Name & Branch : B.Tech (IT)  
 Course Code and Course Name : Computer Architecture and Organization & BITE301L  
 Faculty Name(s) : Dr. Vanitha M, Dr. Deepa M, Dr. Angulakshmi M  
 Class Number(s) : VL2024250502721, VL2024250502716, VL2024250502702  
 Date of Examination : 27.1.25  
 Exam Duration : 90 minutes Maximum Marks: 50

**General instruction(s):**

- Answer All Questions
- M - Max mark; CO - Course Outcome; BL - Blooms Taxonomy Level (1 - Remember, 2 - Understand, 3 - Apply, 4 - Analyse, 5 - Evaluate, 6 - Create)
- Course Outcomes  
 [CO1-Elucidate the arithmetic operations, addressing modes and the performance of computers  
 CO3-Analyse the arithmetic algorithms to perform ALU operations]

| Q.No. | Question                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | M                              | CO  | BL  |
|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------|-----|-----|
| 1.    | <p>(a) Describe the steps involved in executing the machine instruction. <b>SUB R0, LOCA</b> Detailing the transfer between components and the simple control commands required. Assume the instruction is stored at memory location INSTR and the address INSTR is initially held in the PC(Program counter).</p> <p>(b) Convert the following pairs of decimal numbers to 5-bit 2's complement numbers, and then add them. State whether or not overflow occurs in each case.</p> <p>i) -4 and 8</p> <p>ii) -9 and -14</p>                                                                                                  | 6<br><br><br><br><br><br><br>4 | CO1 | BL2 |
| 2.    | <p>(a) Consider a 6 GHz CPU in which data processing (arithmetic and logical) instructions take 6 clock cycles for execution and data transfer (load and store) instructions take 10 clock cycles for execution. When a specific program of 2 million instructions run, 60% of the instructions are data processing and 40% of the instructions are data transfer. Calculate the total time taken to run this program.</p> <p>(b) Explicate with neat sketch on how the operating system overlaps processing, disk transfers, and printing for several programs to make the best possible use of the resources available.</p> | 7<br><br><br><br><br><br><br>3 | CO1 | BL3 |
| 3.    | <p>(a) Represent the integer 1342 in Big Endian and Little Endian machines (32-bit).</p> <p>(b) Write the differences between CISC machine and RISC machine.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 6<br><br><br><br>4             | CO1 | BL3 |

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|    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |    |     |     |
|----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|-----|-----|
| 4. | <p>Write a program to evaluate the arithmetic statement.</p> $Y = (P * Q * R) / (W + S)$ <ul style="list-style-type: none"><li>•Using a general register computer with three address instructions.</li><li>•Using a general register computer with two address instructions.</li><li>•Using an accumulator type computer with one address instructions.</li><li>•Using a stack organized computer with zero-address operation instructions.</li></ul> <p>Where P, Q, R, W, S and Y are memory addresses. In accordance with programming language practice, computing the expression should not change the original value of its operands.</p> | 10 | CO3 | BL3 |
| 5. | <p>Register R1 and R2 of a computer contains the decimal values 4000 and 5600. Base Register BX contains 1500 and index register XR contain 2000. Identify the effective address of the memory operand and also identify the type of addressing modes in each of the following instructions.</p> <ul style="list-style-type: none"><li>i) Load R1, 85 (R2)</li><li>ii) Mov #5600, R3</li><li>iii) Store 90 (R1, R2), R5</li><li>iv) Add (R1) +, R4</li><li>v) SUB - (R2), R5</li><li>vi) Add 5000, R6</li><li>vii) MUL R2, R1</li><li>viii) INC</li><li>ix) Mov R1, [BX] 2400</li><li>x) Mov R1, [XR] 2400</li></ul>                          | 10 | CO1 | BL3 |

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