



VIT

Vellore Institute of Technology

Final Assessment Test – November/December 2023

Course: BECE206L - Analog Circuits

Class NBR(s): 2287 / 2289 / 2291 / 2293 / 2297 / 2299

Slot: G1+TG1

Time: Three Hours

Max. Marks: 100

KEEPING MOBILE PHONE/SMART WATCH, EVEN IN 'OFF' POSITION, IS TREATED AS EXAM MALPRACTICE

Answer ALL Questions

(10 X 10 = 100 Marks)

1. Analyze the following CS Amplifier and draw the small signal circuit and derive the expression for mid-band gain and input impedance R_{in} . Assume presence of channel length modulation. ($\lambda \neq 0$)

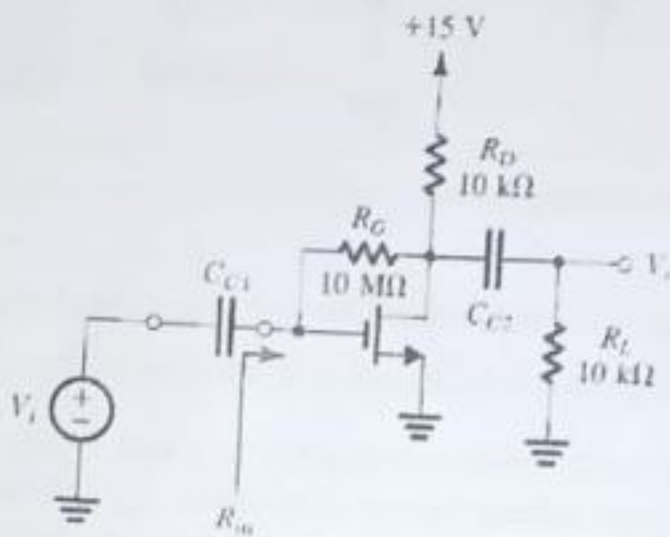


Fig.1 CS Amplifier

- 2.(a) An amplifier with fixed bias has $R_B = 50 \text{ k}\Omega$, $R_C = 500 \Omega$ and $V_{CC} = 12 \text{ V}$. Draw the DC equivalent circuit. Find the coordinates of the operating point. Draw the DC load line and locate the Q-point on the load line. Assume silicon transistor with $\beta = 75$ and $V_{BE} = 0.7 \text{ V}$.

OR

- 2.(b) An enhancement NMOS transistor is connected in the bias circuit of Fig.2, with $V_G = 4 \text{ V}$ and $R_S = 2 \text{ k}\Omega$. The transistor has $V_t = 1 \text{ V}$ and $k_n = 2 \text{ mA/V}^2$. What bias current results? If a transistor for which k_n is 50 % higher is used, what is the resulting percentage increase in I_D ?



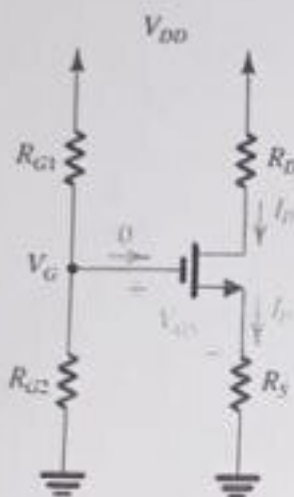


Fig.2 NMOS Voltage Divider Bias Circuits

3. For a class B amplifier using a supply of $V_{DD} = 12\text{ V}$ and driving a load of $8\ \Omega$, determine (i) maximum load power (ii) d.c. input power (iii) collector efficiency.
4. It is required to design an NMOS differential amplifier as shown in Fig.3, to operate with a differential input voltage that can be as high as $v_{id} = 0.3\text{ V}$ while keeping the nonlinear term under the square root in i_{D1} to a maximum of 50 mA . A transconductance $g_m = 1\text{ mA/V}$ is needed. Find the required values of V_{ov} , I , W/L . Assume that the technology available has $\mu_n C_{ox} = 200\ \mu\text{A/V}^2$. What differential gain A_d results for single ended output when $R_D = 10\text{ k}\Omega$? Assume $\lambda = 0$. What is the resulting output signal corresponding to v_{id} at its maximum value?

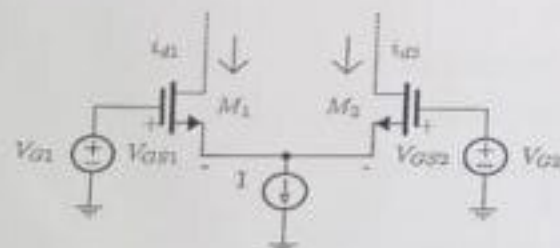


Fig.3 NMOS differential amplifier

5. Consider the NMOS differential pair illustrated in Fig.4, under the conditions that $I = 100\ \mu\text{A}$, using FETs for which $k_n(W/L) = 400\ \mu\text{A/V}^2$, and $V_{th} = 1\text{ V}$. What is the voltage on the common-source connection for $V_{G1} = V_{G2} = 2\text{ V}$? What is the relation between the drain currents (i.e., $i_{D1} - i_{D2}$) in each of these situations (neglect the nonlinear term in drain currents)? Now for $V_{G2} = 0\text{ V}$, at what voltages must V_{G1} be placed to reduce i_{D2} by 10%? To increase i_{D2} by 10%?

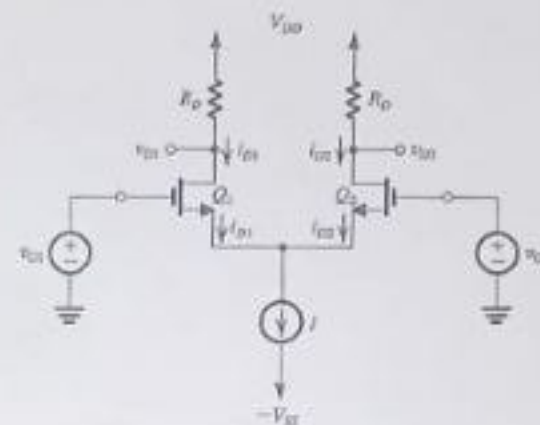


Fig.4 NMOS differential pair

6. Derive the expression for voltage gain of an instrumentation amplifier using op-amps. Justify how the input impedance is improved in the instrumentation amplifier.
7. Determine the output voltage of the circuit shown in Fig. 5. Given $R_1 = 10\text{ k}\Omega$, $R_2 = 20\text{ k}\Omega$, $R_3 = 15\text{ k}\Omega$, $R_4 = 15\text{ k}\Omega$, $R_5 = 30\text{ k}\Omega$, $R_6 = 75\text{ k}\Omega$, $V_1 = 0.1\text{ V}$, $V_2 = 0.2\text{ V}$, $V_3 = 0.3\text{ V}$, and $V_4 = 0.4\text{ V}$.

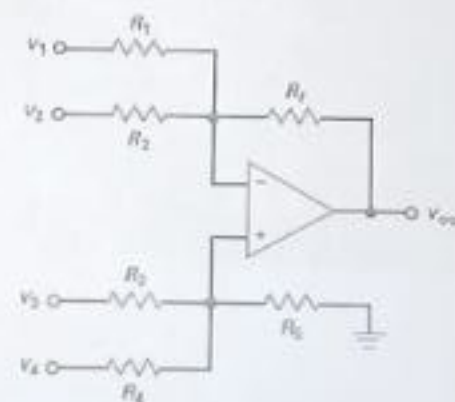


Fig.5.

- 8.(a) With neat sketch explain the operation of Wein-bridge oscillator.

OR

- 8.(b) Explain the operation of Parallel Flash ADC with neat sketch.

9. Design a second order Butterworth low pass filter with a cut off frequency of 1 kHz and input capacitance of $0.01\ \mu\text{F}$. Illustrate the operation of filter with a frequency response plot.

10. Explain the working principle of an Astable multivibrator using IC555 Timer with neat diagram.