

**VIT**Vellore Institute of Technology
(Approved as an Institute under section 3 of the UGC Act, 1956)**Final Assessment Test – April 2023**Course: **BCSE205L - Computer Architecture and Organization**Class NBR(s): **2972/4131**Slot: **A2+TA2**Time: **Three Hours**Max. Marks: **100**Faculty Name: **Prof. AJITHA D****Prof. VENKATA PHANIKRISHNA B****KEEPING MOBILE PHONE/SMART WATCH, EVEN IN "OFF" POSITION, IS TREATED AS EXAM MALPRACTICE****Answer any TEN Questions****(10 X 10 = 100 Marks)**

1. a) Compare Harvard (MARK I) and Von Neumann's architecture. In which context Harvard architecture better than von Neumann architecture? [4]
b) Explain in detail IAS Computer Architecture along with its specifications. [6]
2. Iterate the steps involved in register solving for modified Booths technique with detailed Algorithm (27*-11). (Note: Specify the Algorithm separately)
3. Explain about IEEE-754 Floating-Point Standards with neat diagram? Represent - 12.62510 in either single precision and double precision IEEE-754 format.
4. a) For the expression given $V = (W+X)/Y-Z$ write the instruction using [4]
i. 3-Address
ii. 1-Address
b) For part A instruction created for 3 & 1 address identify the total memory [6]
required to store an Instruction, Memory Required to Encode an Instruction, and Memory Accesses to fetch Instruction and Execute an Instruction.
(Note: system took 3 bytes for both opcode and operand to store. And take 1Byte for opcode and 3 bytes for operand in case of Encoding.)
5. a) Consider the execution of a program which results in the execution of 2 million [5]
instructions on a 400-MHz processor. The instruction mix and the CPI for each instruction type are given in below the table.
Compute MIPS (Million Instructions Per Second) Rating using given data.

Instruction Type	CPI	Instruction Mix
Arithmetic and Logic	1	60%
Load/Store with cache hit	2	18%
Branch	4	12%
Memory reference with cache miss	8	10%

- b) Define Amdahl's Law? A program's 40% code improvement runs 2.3 times [5]
quicker than the original version. What is the system speedup S?

6. Design $2K \times 8$ – bit RAM using 1024×8 – bit RAM chips and $2K \times 8$ – bit ROM using 2048×4 – bit ROM chips
 - a) How many RAM and ROM chips are required? [3]
 - b) How many lines of the address lines required to access 2048 bytes of RAM and 2048 bytes of ROM? How many of these lines will be common to all chips? [3]
 - c) Give the address range in hexadecimal for RAM, ROM. [4]
7.
 - a) What is the difference between the Look through and Look aside cache? [4]
 - b) Suppose that the hit ratio for reads is 90%, which (Look through and Look aside cache) would have the better average access time if cache with an access time of 10ns and a main memory with a cycle time of 100ns? [6]
8. What are the different Data Transfer Modes between the central computer (CPU or Memory) and peripherals? Explain Direct Memory Access (DMA) in detail?
9. Do the RAID levels will increase the performance? Justify in which level and how with a neat sketch in detail.
10. List hazards in the Pipelining process and explain in detail with suitable example.
11. What is parallel computing? Explain Flynn's taxonomy of parallel machine models with a neat diagrams?
12. Explain the reasons for including cache memory in the memory hierarchy? Compare all cache mapping methods using a table?

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