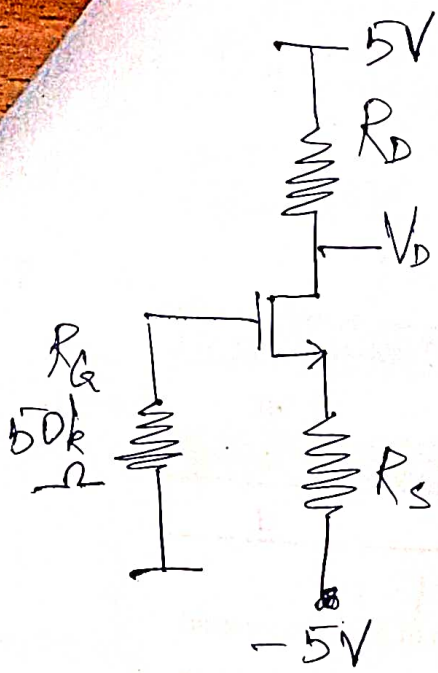
cut-off

* Design a MOSFET circuit biased with positive and negative voltages to meet a set of specifications

→ Design the circuit such as $I_{DQ} = 0.5mA$; $V_{DSQ} = 4V$

$K_n = 0.25 mA/V^2$; $V_{TN} = 1.2V$



Since

$$I_D = K_n (V_{GS} - V_{TN})^2$$

$$V_{GS} = V_{TN} + \sqrt{\frac{I_D}{K_n}} = 1.2 + \sqrt{\frac{0.5}{0.25}}$$

$$= 2.614\,V$$

$$V_{GS} = V_G - V_S = -V_S = 2.614\,V$$

$$V_S = -2.614\,V$$

$$R_S = \frac{-2.614-(-5)}{I_D} = \frac{5-2.614}{0.5}$$

$$\doteq 4.77\,k\Omega$$

$$V_D = V_{DS} + V_S = -2.614+4 = 1.386\,V$$

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{5-1.386}{0.5} = 7.23\,k\Omega$$

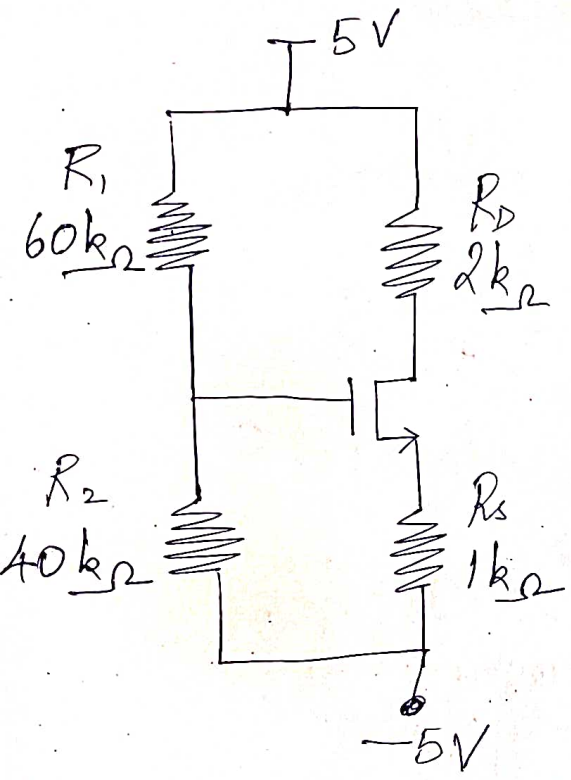
Since ~~$V_{DS} > V_t$~~

$$V_{DS} = 4\,V \Rightarrow V_G - V_T = 2.61 - 1.2$$

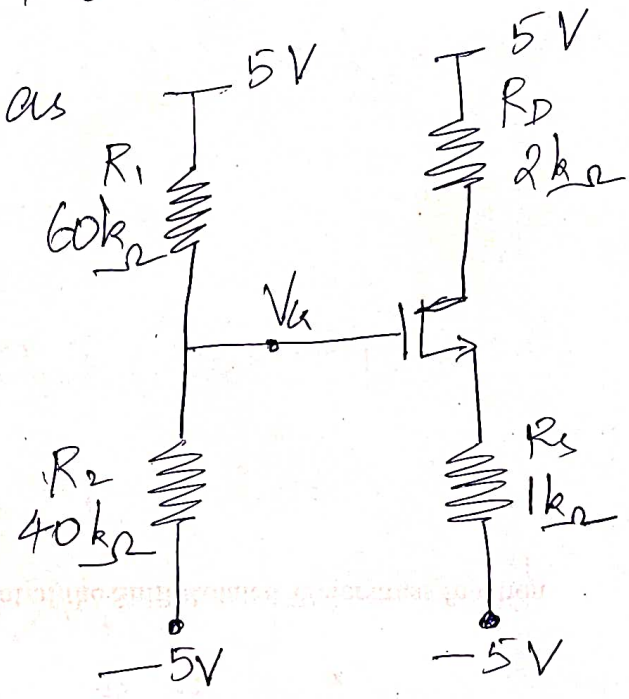
$$= 1.41\,V$$

Our assumption is justified and device is in Saturation region.

For the transistor in the circuit below the parameters are $V_{TN} = 1V$ and $K_n = 0.5 mA/V^2$. Determine V_{GS}, V_{DS} and I_D.



The circuit can be redrawn as



$$V_G = \frac{R_2 V_{DD} + R_1 V_{SS}}{R_1 + R_2} = \frac{-5 \times 60k + 5 \times 40k}{100k}$$

$$= -1V$$

Applying KVL at input loop we get

$$V_G = V_{GS} + I_D R_S + V_{SS}$$

$$= V_{GS} + K_n (V_{GS} - V_{TN})^2 R_S + V_{SS}$$

Assuming saturation.

$$-1 = V_{GS} + 0.5(V_{GS} - 1)^2 - 5$$

$\Rightarrow$ ~~$V_{GS} + V_{GS}^2 - 2V_{GS} + 1 - 5 + 1 = 0$~~.

~~$V_{GS}^2 - V_{GS} - 3 = 0$~~

~~$-1 + V_{GS} + 0.5V_{GS}^2 - V_{GS} + 0.5 + 1 - 5 = 0$~~

~~$0.5V_{GS}^2 =$~~

$$-1 = V_{GS} + 0.5(V_{GS} - 1)^2 - 5$$

$$= 0.5(V_{GS} - 1)^2 + V_{GS} - 4 = 0$$

$$0.5\left[V_{GS}^2 - 2V_{GS} + 1\right] + V_{GS} - 4 = 0$$

$$0.5V_{GS}^2 - V_{GS} + 0.5 + V_{GS} - 4 = 0$$

$$0.5V_{GS}^2 - 3.5 = 0$$

$$V_{GS} = 2.645\ V.$$

$$I_D = K_n(V_{GS} - V_{TN})^2$$

$$= 0.5(2.645 - 1)^2 = 1.354\ mA$$

$$V_{DS} = V_{DD} - I_D R_D - I_S R_S - V_{SS}$$

$$= 5 - I_D (R_S + R_D) - (-5)$$

$$= 10 - I_D (3k) = 5.937\ V$$

We ~~10~~ note that

$$V_{DS} = 5.937 \geq V_{GS} - V_{Tn} = 1.65\ V$$